



OKI.459

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#8
4-29-03
C. Brown

In re PATENT APPLICATION of

Katsuaki Matsui

Group Art Unit: 2857

Serial No.: 09/839,671

Examiner: J. West

Filed: April 23, 2001

FOR: SEMICONDUCTOR DEVICE HAVING A MODE OF FUNCTIONAL TEST

DRAWING CORRECTION APPROVAL REQUEST

Honorable Commissioner of
Patents and Trademarks,
Washington, D.C. 20231

Date: April 22, 2003

Sir:

Applicant respectfully requests the Examiner's approval of the following drawing corrections indicated in red ink on the attached sheets.

In Fig. 1, elements 102, 103, 104 and 105 have been denoted as "SELECTOR".

In Fig. 3, elements 302, 303 and 304 have been denoted as "SELECTOR".

In Fig. 4, elements 404, 405, 406 and 407 have been denoted as "SELECTOR"; element 402 as "LOGIC CIRCUIT BLOCK"; element 402a as "LATCH" and element 403 as "DUMMY LATCH".

In Fig. 5, elements 502, 503, 504 and 505 have been denoted as "SELECTOR".

Corrected formal drawings will be prepared and filed upon approval by the Examiner and subsequent indication of allowance of the present application.


In the event that there are any outstanding matters remaining in the present

application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.


Andrew J. Telesz, Jr.
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AJT:dmc

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Enclosures: Four (4) sheets of red-inked drawings